WHAT IS CLAIMED IS:

1. A method for accommodating transition-induced delay comprising the steps of:

determining a first relationship between a first line current logic state of a first line and a first line next logic state;

adjusting a first delay in the first line based on the first relationship.

2. The method of claim 1 further comprising the step of:

determining a second relationship between a second line current logic state of a second line and a second line next logic state, wherein the step of adjusting the first delay in the first line based on the first relationship further comprises the step of:

adjusting the first delay in the first line based on the first and second relationships.

3. The method of claim 2, wherein the step of adjusting the first delay in the first line based on the first and second relationships further comprises the step of:

adjusting the first delay in the first line and a second delay in the second line based on the first and second relationships.

4. The method of claim 1, wherein the step of adjusting the first delay in the first line based on the first relationship further comprises the step of:

providing less delay when the first line current logic state and the first line next logic state are different than when the first line current logic state and the first line next logic state are similar.

5. A method for accommodating transition-induced delay comprising the steps of:

determining a first relationship between a first line current logic state of a first line and a first line next logic state;

causing a first timing signal to occur at a first time based on the first relationship, wherein the first line is sampled in accordance with the first timing signal.

6. The method of claim 5 further comprising the step of:

adjusting a first delay in the first line based on the first relationship.

7. The method of claim 5, wherein the step of causing the first timing signal to occur at the first time based on the first relationship further comprises the step of:

causing the first time to exhibit different delay when the first line current logic state and the first line next logic state are different than when the first line current logic state and the first line next logic state are similar.

8. Apparatus for accommodating transition-induced delay comprising:

a transition detection block having a plurality of inputs, the inputs coupled to a plurality of lines, the transition detection block detecting transitions of the lines; and

a delay adjustment block coupled to the transition detection block, the delay adjustment block adjusting a delay in at least one of the lines.

9. The apparatus of claim 8, wherein the transition detection block detects a first type of the transitions from a first level to a second level and a second type of the transitions from the second level to the first level.

10. The apparatus of claim 9, wherein the delay adjustment block adjusts the delay based on a relationship between the first type of the transitions and the second type of the transitions.

11. The apparatus of claim 10, wherein the relationship is a difference between a first number of the lines exhibiting the first type of the transitions and a second number of the lines exhibiting the second type of the transitions.

12. Apparatus for accommodating transition-induced delay comprising:

a transition detection block having a plurality of inputs, the inputs coupled to a plurality of lines, the transition detection block detecting transitions of the lines; and

a delay adjustment block coupled to the transition detection block, the delay adjustment block adjusting a delay affecting a timing signal, wherein at least one of the lines is sampled in accordance with the timing signal.

13. The apparatus of claim 12, wherein the transition detection block detects a first type of the transitions from a first level to a second level and a second type of the transitions from the second level to the first level.

14. The apparatus of claim 13, wherein the delay adjustment block adjusts the delay based on a relationship between the first type of the transitions and the second type of the transitions.

15. The apparatus of claim 14, wherein the relationship is a difference between a first number of the lines exhibiting the first type of the transitions and a second number of the lines exhibiting the second type of the transitions.

16. A method for accommodating transition-induced delay comprising the steps of:

detecting transitions on a plurality of lines; and

adjusting a delay in at least one of the plurality of lines based on the transitions on the plurality of lines.

17. The method of claim 16, wherein the step of detecting transitions on the plurality of lines further comprises the steps of:

detecting first-level-to-second-level transitions on the plurality of lines; and

detecting second-level-to-first-level transitions on the plurality of lines.

18. The method of claim 17, wherein the step of adjusting the delay in the at least one of the plurality of lines based on the transitions on the plurality of lines further comprises the step of:

adjusting the delay in the at least one of the plurality of lines based on a difference in respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions.

19. The method of claim 18, wherein the step of adjusting the delay in the at least one of the plurality of lines based on the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions further comprises the step of:

increasing the delay when the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions is decreased.

20. The method of claim 18, wherein the step of adjusting the delay in the at least one of the plurality of lines based on the difference in respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions further comprises the step of:

adjusting the delay differently when there are more of the first-level-to-second-level transitions than when there are more of the second-level-to-first-level transitions.

21. The method of claim 18, wherein the step of adjusting the delay in the at least one of the plurality of lines based on the difference in respective numbers of the first-level-to-second-level

transitions and the second-level-to-first-level transitions further comprises the step of:

adjusting the delay in the at least one of the plurality of lines based on comparison of the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions to a threshold.

22. The method of claim 21, wherein the step of adjusting the delay in the at least one of the plurality of lines based on comparison of the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions to the threshold further comprises the step of:

adjusting the delay in the at least one of the plurality of lines based on comparison of the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions to a plurality of thresholds, with the delay adjusted a different amount for a first threshold of the plurality of thresholds than for a second threshold of the plurality of thresholds.

23. A method for accommodating transition-induced delay comprising the steps of:

detecting transitions on a plurality of lines; and

controlling timing of a timing signal for sampling the plurality of lines based on the transitions on the plurality of lines.

24. The method of claim 23, wherein the step of detecting transitions on the plurality of lines further comprises the steps of:

detecting first-level-to-second-level transitions on the plurality of lines; and

detecting second-level-to-first-level transitions on the plurality of lines.

25. The method of claim 24, wherein the step of controlling timing of a timing signal for sampling the plurality of lines based on the transitions on the plurality of lines further comprises the step of:

controlling the timing of the timing signal for sampling the plurality of lines based on a difference in respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions.

26. The method of claim 25, wherein the step of controlling the timing of the timing signal for sampling the plurality of lines based on a difference in respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions further comprises the step of:

delaying the timing of the timing signal when the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions is increased.

27. The method of claim 25, wherein the step of controlling the timing of the timing signal for sampling the plurality of lines based on a difference in respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions further comprises the step of:

controlling the timing of the timing signal differently when there are more of the first-

level-to-second-level transitions than when there are more of the second-level-to-first-level transitions.

28. The method of claim 25, wherein the step of controlling the timing of the timing signal for sampling the plurality of lines based on a difference in respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions further comprises the step of:

controlling the timing of the timing signal for sampling the plurality of lines based on a comparison of the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions to a threshold.

29. The method of claim 28, wherein the step of controlling the timing of the timing signal for sampling the plurality of lines based on a comparison of the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions to a threshold further comprises the step of:

controlling the timing of the timing signal for sampling the plurality of lines based on comparison of the difference in the respective numbers of the first-level-to-second-level transitions and the second-level-to-first-level transitions to a plurality of thresholds, with the delay adjusted a different amount for a first threshold of the plurality of thresholds than for a second threshold of the plurality of thresholds.

30. The method of claim 24, wherein the step of controlling the timing of the timing signal for sampling the plurality of lines based on the transitions on the plurality of lines further comprises the step of:

controlling the timing of the timing signal for sampling the plurality of lines based on a relationship between respective numbers a first set of the plurality of lines exhibiting first-level-to-second-level transitions, a second set of the plurality of lines exhibiting second-level-to-first-level transitions, and a third set of the plurality of lines exhibiting logic levels remaining unchanged during the first-level-to-second-level transitions of the first set of the plurality of lines and the second-level-to-first-level transitions of the second set of the plurality of lines.

31. The method of claim 30, wherein the timing of the timing signal is later when the third set of the plurality of lines is smaller and earlier when the third set of the plurality of lines is larger.

32. A method for accommodating transition-induced delay comprising the steps of:

detecting conditions on a plurality of lines, wherein the conditions are indicative of the transition-induced delay; and

controlling recovery of information from the plurality of lines by controlling timing of a signal based on the conditions.

33. The method of claim 32, wherein the step of controlling the recovery of the information from the plurality of lines by controlling the timing of the signal based on the conditions further comprises the step of:

controlling the recovery of the information from the plurality of lines by controlling the timing of the signal on at least one of the plurality of lines based on the conditions.

34. The method of claim 32, wherein the step of controlling the recovery of the information from the plurality of lines by controlling the timing of the signal based on the conditions further comprises the step of:

controlling the recovery of the information from the plurality of lines by controlling the timing of the signal on a timing signal line separate from the plurality of lines based on the conditions.

35. The method of claim 32, wherein the conditions are further indicative of current flow through a power supply conductor, the current flow affecting a voltage of the power supply conductor.

36. A method for accommodating delay variation among multiple signals comprising the steps of:

performing a comparison between a signal of the multiple signals to be transmitted on a conductor and other signals of the multiple signals to be transmitted on neighboring conductors; and

adjusting timing based on the comparison.

37. The method of claim 36 wherein the step of adjusting timing comprises the step of:

adjusting timing of a transmit clock signal used to transmit the signal.

38. The method of claim 36 wherein the step of adjusting timing comprises the steps of:

generating a plurality of selectable transmit clock signals; and

using one of the plurality of the selectable transmit clock signals as a transmit clock signal to transmit the signal.

39. The method of claim 38 wherein the step of generating a plurality of selectable transmit clock signals comprises the steps of:

generating a nominal clock signal of nominal clock timing;

generating an early clock signal of earlier phase than the nominal clock signal; and

generating a late clock signal of later phase than the nominal clock signal.

40. The method of claim 36 wherein the step performing a comparison comprises the steps of:

determining a first outcome of the comparison when the other signals to be transmitted on the neighboring conductors are of a similar state as the signal;

determining a second outcome of the comparison when one of the other signals to be transmitted on the neighboring conductors is of a similar state as the signal and another of the other signals to be transmitted on the neighboring conductors is of a different state than the signal; and

determining a third outcome of the comparison when the other signals to be transmitted

on the neighboring conductors are of a different state than the signal.

41. The method of claim 40 wherein the step of adjusting timing further comprises the steps of:

using a nominal timing when the comparison has the second outcome;

using an earlier timing when the comparison has the first outcome; and

using a later timing when the comparison has the third outcome.

42. The method of claim 40 wherein the step of adjusting timing further comprises the steps of:

delaying the signal by a nominal amount when the comparison has the second outcome;

delaying the signal by a smaller than nominal amount when the comparison has the first outcome; and

delaying the signal by a larger than nominal amount when the comparison has the third outcome.

43. The method of claim 36 wherein the step of adjusting timing comprises the step of:

adjusting a delay of the signal.

44. Apparatus for accommodating delay variation among multiple signals comprising:

a clock generation circuit for generating a plurality of selectable clock signals;

a pattern identification logic circuit for comparing a signal of the multiple signals to other signals of the multiple signals to be transmitted on neighboring conductors; and

a clock selection circuit for selecting among the plurality of selectable clock signals based on an output of the pattern identification logic circuit.

45. The apparatus of claim 44 wherein the plurality of selectable clock signals comprise a nominal clock signal of nominal timing, an early clock signal of earlier phase than the nominal clock signal, and a late clock signal of later phase than the nominal clock signal.

46. The apparatus of claim 45 wherein the clock selection circuit selects the early clock signal when the other signals are of a similar state as the signal.

47. The apparatus of claim 45 wherein the clock selection circuit selects the late clock signal when the other signals are of a different state than the signal.

48. The apparatus of claim 45 wherein the clock selection circuit selects the nominal clock signal when one of the other signals is of a similar state as the signal and another of the other signals is of a different state than the signal.

49. The apparatus of claim 44 wherein the clock selection circuit comprises a multiplexer.

50. Apparatus for accommodating delay variation among multiple signals comprising:

a pattern identification logic circuit for comparing a signal of the multiple signals to other signals of the multiple signals to be transmitted on neighboring conductors; and

a delay circuit for delaying the signal based on an output of the pattern identification logic circuit.

51. The apparatus of claim 50 wherein the output of the pattern identification logic circuit is indicative of a first outcome when the other signals to be transmitted on the neighboring conductors are of a similar state as the signal, a second outcome when one of the other signals to be transmitted on the neighboring conductors is of a similar state as the signal and another of the other signals to be transmitted on the neighboring conductors is of a different state than the signal, and a third outcome when the other signals to be transmitted on the neighboring conductors are of a different state than the signal.

52. The apparatus of claim 51 wherein the delay circuit delays the signal by a nominal amount when the output indicates the second outcome, by a smaller than nominal amount when the output indicates the first outcome, and by a larger than nominal amount when the output indicates the third outcome.